CoaXPress IP Core

COAXPRESS IP CORE FOR FPGA

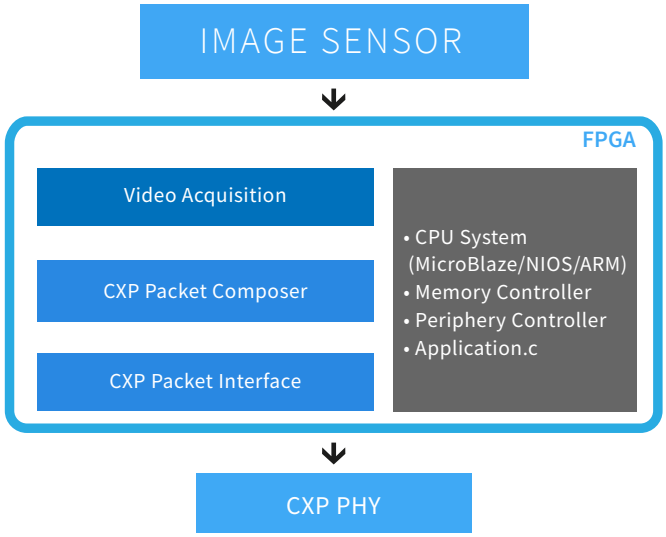
AT A GLANCE

- Compatible with Xilinx 7 Series (and higher) and Intel Cyclone V devices (and higher)
- Compact, customizable
- Speed support from 1 Gb/s to more than 50 Gb/s
- Delivered with a working reference design

CoaXPress is a standard communication protocol for vision applications based on widely used coaxial cables. It allows easy interfacing between cameras and frame grabbers and supports the GenICam software standard. Sensor to Image offers a set of IP cores and a development framework to build FPGA-based products using the CoaXPress interface. Due to the speed of CXP, senders and receivers require a fast FPGA-based implementation of the CXP core, preferably using embedded transceivers. CXP cores are compatible with Xilinx 7 series devices (and higher) and Intel/Altera Cyclone V devices (and higher).

Working Reference Design

Sensor to Image CXP FPGA solution is delivered as a **working reference design** along with FPGA IP cores. This minimizes development time and allows for top-notch performance at a small footprint, while leaving enough flexibility to customize the design. Sensor to Image cores are compact and leave enough space in the FPGA for your application.



Top Level Design

The first component of the IP Core is the **Top Level Design**. It is an interface between external hardware (imager, sensors, CXP PHY) and FPGA internal data processing. We deliver this module as VHDL source code that can be adapted to custom hardware.

Video Acquisition Module

The **Video Acquisition Module** of the reference design simulates a camera with a test pattern generator. This module is delivered as VHDL source code, which has to be replaced by a sensor interface and pixel processing logic in the camera design.

CoaXPress Streaming Interface

The **CXP Streaming Interface** receives all data from the video sensor output to the CXP PHY. It reaches the full speed on the streaming channel according to the CXP specification.

CoaXPress Control Interface

The **CXP Control Interface** receives and sends all data from the CXP control channel, from and to the CXP PHY and implements the control channel according to the CXP specification.

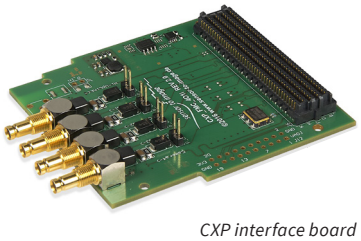
FPGA Integrated CPU

An **FPGA integrated CPU** (MicroBlaze, NIOS, ARM) is used for several non-time-critical control and configuration tasks on the CXP-receiver or transmitter core. This software is written in C and can be extended by the customer.

Custom Configuration

Some parts of the design are compiled files only (for example the CXP control protocol library), while other parts are source code. The design framework comes with all the necessary design files and cores, Vivado or Quartus project files. It is configured either as a CXP camera system with an optional CMOS imager, or as an embedded CXP host (receiver). This system is used as a **reference design** and **evaluation board**. The reference design uses the Xilinx or Intel development tools (not in the scope of delivery).

Sensor to Image **MVDK development kit** is a flexible evaluation platform for machine vision applications. It supports CoaXPress host and device reference designs and various Enclustra™ FPGA modules with Intel and Xilinx FPGAs.



CXP interface board

AVAILABLE MODULES

MODULE	DESCRIPTION	ZYNQ7	KINTEX ULTRASCALE	MPSOC	CYCLONE -10
Video Acquisition Interface (Device)	Simple CMOS imager interface or test pattern generator	•	•	•	•
CXP Packet DeComposer (Host Core)	CoaXPress streaming protocol packet receiver				
Encrypted VHDL		•	•	•	•
VHDL source		o	o	o	o
CXP Packet Composer (Device Core)	CoaXPress streaming protocol packet composer				
Encrypted VHDL		•	•	•	•
VHDL source		o	o	o	o
CXP12 Speed Support	Support for CXP12 with 64bit pixel interface	o	o	o	o
FPGA CPU CoaXPress application source	CoaXPress user application	•	•	•	•
FPGA CPU CoaXPress library	CoaXPress control protocol library				
Object file		•	•	•	•
C-sources		o	o	o	o

RESOURCE USAGE

MODULE	ZYNQ7	KINTEX ULTRASCALE	MPSoC	CYCLONE -10
Top Level and Video aquisition interface - Test pattern generator				
Registers	473	445	445	575
Lookup Tables	338	290	288	579
BlockRAMs	0	0	0	1
CPU System -µBlaze/ARM/NIOS based CPU system				
Registers	987	3051	835	3621
Lookup Tables	708	3236	558	3663
BlockRAMs	0	16	0	42
DSP	0	3	0	3
CXP Packet composer (Device Core)				
Registers	9794	9701	11640	11152
Lookup Tables	7829	7606	9109	11461
BlockRAMs	15	15	15	60
DSPs	4	4	4	4
GigE Vision Packet composer - GigE Vision streaming protocol packet composer				
Registers	6394	6280	8722	8722
Lookup Tables	5297	5159	7171	7171
BlockRAMs	18	18	18	18
Transceiver	4	4	4	4

LEGEND

Included	•
Optional	o
Please contact us	-