GigE Vision IP Core

GIGE VISION IP CORE FOR FPGA

AT A GLANCE

- Compatible with Xilinx 7 Series (and higher) and Intel (Altera Cyclone V devices (and higher)
- Compact, customizable
- Speed support from 100 Mb/s to more than 10 Gb/s
- Delivered with a full featured reference design

GigE Vision is a standard communication protocol for vision applications based on the well-known Ethernet technology. It allows easy interfacing between GigE Vision devices and PCs running TCP/IP protocol family. Sensor to Image offers a set of IP cores and a development framework to build FPGA-based products using the GigE Vision interface. Due to the speed of GigE Vision, especially at speeds higher than 1 Gb/s, senders and receivers require a fast FPGA-based implementation of the embedded GigE core. GigE Vision cores compatible with Xilinx 7 Series devices (and higher) and Intel/Altera Cyclone V devices (and higher).

Working Reference Design

Sensor to Image GigE Vision FPGA solution is delivered as a **working reference design** along with FPGA IP cores. This minimizes development time and allows for top-notch performance at a small footprint, while leaving enough flexibility to customize the design. Sensor to Image cores are compact and leave enough space in the FPGA for your application.

Top Level Design

The first component of the IP Core is the **Top Level Design**. It is an interface between external hardware (imager, sensors, GigE PHY) and FPGA internal data processing. We deliver this module as VHDL source code that can be adapted to custom hardware.

Video Acquisition Module

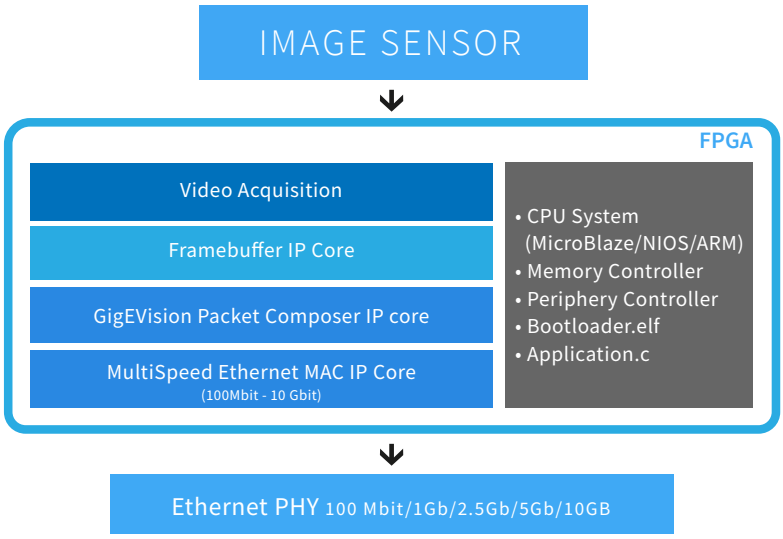
The **Video Acquisition Module** of the reference design simulates a camera with a test pattern generator. This module is delivered as VHDL source code, which has to be replaced by a sensor interface and pixel processing logic in the camera design.

Framebuffer

The **Framebuffer** core interfaces to the FPGA vendor specific memory controller. The framebuffer allows frame buffering and image partitioning. This is necessary to implement the GigE Vision packet resend function.

GigE Packet Composer

The **GigE Packet Composer** sends all data to the Ethernet MAC and implements the high-speed GigE Vision Streaming Protocol (GVSP).



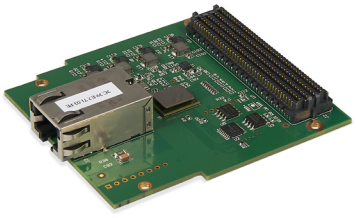
FPGA Integrated CPU

An **FPGA integrated CPU** (MicroBlaze, NIOS, ARM) handles non-time-critical network and configuration tasks and runs the GigE Vision Control Protocol (GVCP). This software is written in C and can be extended by the customer.

Custom Configuration

Some parts of the design are delivered as compiled files only (for example the GigE Vision control protocol library), while other parts are delivered as source code. The design framework comes with all the necessary design files and cores, Vivado or Quartus project files. It is configured either as a GigE Vision camera system with an optional CMOS imager, or as an embedded GigE Vision host (receiver). This system is used as a **reference design** and **evaluation board**. The reference design uses the Xilinx or Intel development tools (not in the scope of delivery).

Sensor to Image **MVDK development kit** is a flexible evaluation platform for machine vision applications. It supports GigE Vision host and device reference designs and various Enclustra™ FPGA modules with Intel and Xilinx FPGAs.



NBASE-T interface board

AVAILABLE MODULES

MODULE	DESCRIPTION	ARTIX-7	ZYNQ-7	MPSoC	CYCLONE-5
Video Acquisition Interface (Device)	Simple CMOS imager interface or test pattern generator	•	•	•	•
FB-AXI encrypted VHDL (Device)	External memory based streaming buffer, uses Xilinx or Intel AXI memory controller	•	•	•	•
Framebuffer Linesscan support	Support of variable blocksizes often used in linescan applications	o	o	o	o
GigE Vision Packet DeComposer encrypted VHDL (Host)	GigE Vision streaming protocol packet receiver	•	•	•	•
GigE Vision Packet Composer encrypted VHDL (Device)	GigE Vision streaming protocol packet composer	•	•	•	•
TRI Mode MAC encrypted VHDL	10/100/1000 Mbit/s Ethernet MAC	•	•	•	•
10G MAC encrypted VHD	2,5/5/10Gbit/s Ethernet MAC	o	o	o	o
IEEEE1588 Support (Device)	Support for the IEEE1588 time synchronisation protocol	o	o	o	o
ACTION Command	Support for low latency GigE Vision Action command encoder and decoder	o	o	o	o
Multipart Frontend (Device)	Support of GigE Vision Multipart Payload Type	o	o	o	o
FPGA CPU Bootloader	GigE Vision bootloader application				
Object file		•			•
C-source		o			o
FPGA CPU GigE Vision application source	GigE Vision user application	•	•	•	•
FPGA CPU GigE Vision library	GigE Vision control protocol library				
Object file		•	•	•	•
C-source		o	o	o	o
FPGA CPU Linux driver	Linux driver for the GigE Vision core	o	o	o	o

RESOURCE USAGE

MODULE	ARTIX-7	ZYNQ-7	MPSoC	CYCLONE-5
Top Level and Video aquisition interface - Test pattern generator				
Registers	595	555	661	596
Lookup Tables	487	308	441	564
BlockRAMs	0	0	0	0
CPU System -µBlaze/ARM/NIOS based CPU system with AXI memory controller				
Registers	9177	1392	890	4448
Lookup Tables	10389	1031	596	4068
BlockRAMs	10	0	0	10
DSP	3	0	0	3
FB-AXI - External memory based streaming buffer, uses Xilinx or Intel AXI memory controller				
Registers	5747	5901	5843	4615
Lookup Tables	4203	4333	4203	3167
BlockRAMs	11	15	11	15
DSPs	1	1	1	1
GigE Vision Packet composer - GigE Vision streaming protocol packet composer				
Registers	4808	4681	4701	5221
Lookup Tables	2925	2842	2705	3377
BlockRAMs	9	9	9	9
Tri Mode Ethernet MAC				
Registers	1224	1224	1224	1204
Lookup Tables	868	867	868	729
BlockRAMs	3	5	3	4

GIGE VISION HOST SOFTWARE

SOFTWARE MODULE	WIN7	WIN10	LINUX (UBUNTU LTS)	MAC OS
GigE Vision filter driver				
No sources	•	•	o	o
C-sources	o	o	o	o
GigE Vision library				
Object file	•	•	o	o
C-sources	o	o	o	o
GigE Vision Sphinx Viewer application				
C-sources	•	•	o	o

LEGEND

Included	•
Optional	o
Please contact us	-