USB3 Vision IP Core

USB3 VISION IP CORE FOR FPGA

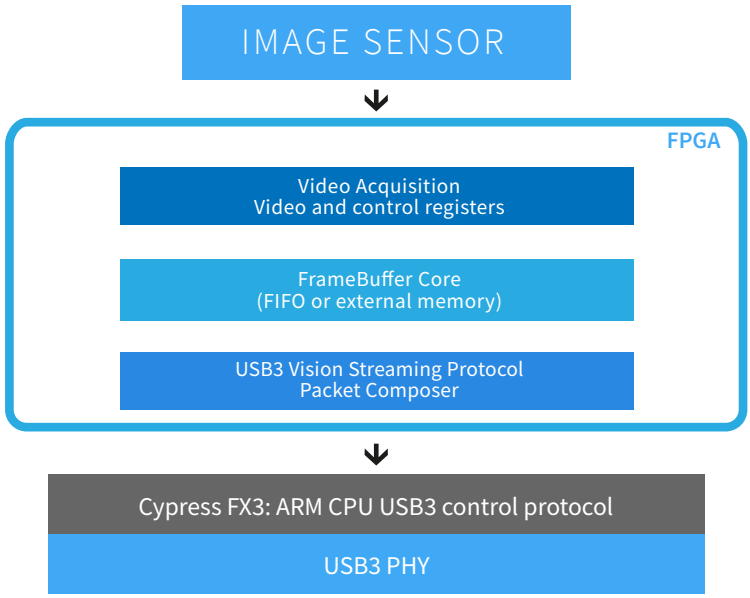
AT A GLANCE

- Compatible with Xilinx 7 Series (and higher) and Intel Cyclone V devices (and higher)
- Compact, customizable
- Delivered with a working reference design

USB3 Vision is a standard communication protocol for vision applications based on the widely used USB 3.0 interface. As the protocol is standard and supports GenICam, it allows easy interfacing between cameras and PCs. Sensor to Image offers a set of IP cores and a development framework to build FPGA-based products using the USB3 Vision interface. Due to the speed of USB3 Vision, senders and receivers require a fast FPGA-based implementation of the embedded USB core. USB3 Vision cores compatible with Xilinx 7 Series devices (and higher) and Intel/Altera Cyclone V devices (and higher).

Working Reference Design

Sensor to Image USB3 Vision FPGA solution is delivered as a **working reference design** along with FPGA IP cores. This minimizes development time and allows for top-notch performance at a small footprint, while leaving enough flexibility to customize the design. Sensor to Image cores are compact and leave enough space in the FPGA for your application.



Top Level Design

The first component of the IP Core is the **Top Level Design**. It is an interface between external hardware (imager, sensors, USB3 PHY) and FPGA internal data processing. We deliver this module as VHDL source code and it can be adapted to custom hardware.

Video Acquisition Module

The **Video Acquisition Module** of the reference design simulates a camera with a test pattern generator. This module is delivered as VHDL source code, which is easily replaced by a sensor interface and pixel processing logic in the camera design.

USB3 Vision Streaming Protocol Packet Composer

The **USB3 Vision Streaming Protocol Packet Composer** takes all data from the video source and builds the USB3 Vision streaming packets. It also handles all low-level communication to the USB3 PHY.

Framebuffer Core

The **Framebuffer core** interfaces to the FPGA vendor specific memory controller. The framebuffer is used for leveling out communication delays between camera and PC.

Cypress FX3

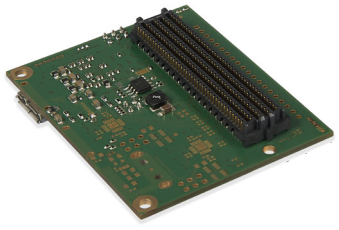
A **Cypress FX3** chip (with integrated ARM CPU and physical interface) is used to handle all USB3 initialization routines and USB3 Vision control channel communication.

Custom Configuration

Some parts of the design are compiled files only (for example the USB3 Vision control protocol library), while other parts are source code. The design framework comes with all the necessary design files and cores, Vivado or Quartus project files. It is configured as a USB3 Vision camera system with an optional CMOS imager.

This system is used as a **reference design** and **evaluation board**. The reference design uses the Xilinx or Intel development tools (not in the scope of delivery).

Sensor to Image **MVDK development kit** allows is flexible evaluation platform for machine vision applications. It supports USB3 Vision device designs and various Enclustra™ FPGA modules with Intel and Xilinx FPGAs.



USB3 interface board

AVAILABLE MODULES

MODULE	DESCRIPTION	ARTIX-7	ZYNQ-7	CYCLONE-5
Video aquisition interface	Simple CMOS imager interface or test pattern generator	•	•	•
FB-FIFO	BlockRAM based streaming buffer			
Encrypted VHDL		•	•	•
VHDL source		o	o	o
FB-AXI encrypted VHDL	External memory based streaming buffer, uses Xilinx or Intel AXI memory controller	o	o	o
USB3 Vision Packet composer	USB3 Vision streaming protocol packet composer			
Encrypted VHDL		•	•	•
VHDL source		o	o	o
FX3 USB3 Vision application sources	USB3 Vision user application	•	•	•
FX3 USB3 Vision library	USB3 Vision control protocol library			
Object file		•	•	•
C-sources		o	o	o

RESOURCE USAGE

MODULE	ARTIX-7	ZYNQ-7	CYCLONE-5
Top Level and Video aquisition interface - Test pattern generator			
Registers	622	623	679
Lookup Tables	381	424	551
BlockRAMs	0	0	0
CPU System - µBlaze/ARM/NIOS based CPU system with AXI memory controller			
Registers	7642	1897	3523
Lookup Tables	8864	1564	3341
BlockRAMs	6	1	49
DSP	3	0	3
FB-FIFO - BlockRAM based streaming buffer (64kB)			
Registers	1892	1890	2038
Lookup Tables	811	808	1077
BlockRAMs	16	16	64
DSP	5	5	4
FB-AXI - External memory based streaming buffer, uses Xilinx or Intel AXI memory controller			
Registers	4360	4326	4615
Lookup Tables	3296	3284	3167
BlockRAMs	6	6	15
USB3 Vision Packet composer - USB3 Vision streaming protocol packet composer			
Registers	2743	2727	2936
Lookup Tables	2127	2117	2386
BlockRAMs	1	1	4

USB3 VISION HOST SOFTWARE

SOFTWARE MODULE	WIN7	WIN10	LINUX (UBUNTU/LTS)	MAC OS
USB3 Vision driver				
No sources	•	•	o	-
C-sources	o	o	o	-
USB3 Vision library				
Object file	•	•	o	-
C-sources	o	o	o	-
USB3 Vision Sphinx Viewer application				
C-sources	•	•	o	-

LEGEND

Included	•
Optional	o
Please contact us	-